TIMOTHY COYLE

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Location: Bangor, ME

HARDWARE ENGINEER

Hardware Engineer with over 15 years experience in hardware development and embedded design from prototype to large scale production in semiconductor and consumer electronic market segments. Technical leader/manager with small teams. Strong background in high-speed digital design for Signal Integrity and EMC design and analysis.

Skills

PCB DESIGN
PCB Schematics, Layout, Lab Debugging

Signal Integrity/EMC
EMSCAN, 3D Simulation and Modeling, Power Integrity, PDN Design, IBIS, Transmission Line Analysis/Crosstalk

EDA CAD/SIMULATION TOOLS
Cadence Allegro/Orcad, Sigrity Speed2K, Mentor Graphics HyperLynx, Agilent ADS, Ansys Designer/SiWave/HFSS, HSPICE, PSPICE, PADS, EagleCAD, Matlab, IBIS Modeling (SPICE to IBIS Conversion), LabView, Python, VBA, C/C++

HARDWARE RF/EMBEDDED DESIGN
Embedded software, Microcontrollers, FPGA, Digital Circuits, DDR/LPDDR, Arduino, Antenna Design, Software Defined Radio

Management/Business/Communication
Technical leader, Experienced Manager

Work Experience

HARDWARE ENGINEER/FOUNDER – Signal Bytes Technology – Bangor, ME – Nov 2015 – Present
Provide hardware and software engineering design services to clients in multiple areas including Microwave RF, Embedded System, Digital Signal Processing, Signal Integrity, and Software Development. Develop and productize/license new technologies in consumer electronic market.

PRINCIPAL HARDWARE ENGINEER – Broadcom - Andover, MA – Jan 2013 – Nov 2015
Individual technical contributor supporting all hardware design aspects of DDR PHY development within company including EMC. Work in hardware engineering group with focus on low-cost consumer designs including 2 and 4 Layer PCB designs.

- Supporting DDR2/DDR3/DDR4 and LPDDR3/LPDDR4. Support internal and external customers.
- Tasks include PCB stackup design, layout review, Signal/Power Integrity/EMC simulation, lab verification and correlation.
- Evaluation on DRAMs to support memory controller including chip ballout, breakout routing studies, and protocol/functional verification for JEDEC memory compliance.
- Current focus on research and development with projects including: PCB decap reduction through PDN analysis, Automated DDR3 waveform/timing validation in HyperLynx, EMI 3D simulation to correlation with EMSCAN

DIRECTOR OF HARDWARE ENGINEERING – Signal Consulting Group LLC – Portland, ME – Jan 2008 – Dec 2012
Managed small team of software and hardware engineers overseeing client projects. Provided business and technical solutions for various hardware design projects. Subject Matter Expert on Signal Integrity and EMC including patent analysis work.

- Developed and licensed PCB CAD application for Signal Integrity to clients in semiconductor industry and grew software sales to 25% of total company revenue in 2 years. Led software development in Java language for enterprise software market while managing two software developers.
- Created training program for engineers on Signal Integrity and delivered on-site training to Fortune 500 clients across the globe and introduced eLearning video format with screen capture technology to further increase client base. Designed and launched a digital magazine for hardware engineering industry that included technical articles authored by industry leaders and published four issues that generated over 3000 downloads per issue.
- Performed Signal Integrity and EMC analysis on numerous client projects as technical lead and Subject Matter Expert (SME). Managed PCB design and layout engineers for client projects.

SENIOR HARDWARE DESIGN ENGINEER – IDT – Portland, ME – Sept 2006 – Jan 2008

Design and support for product line of interface chips including PCI, PCI-Express, RapidIO, Ethernet, and DDR2/3. Worked with other board designers and architects to evaluate system protocol efficiency and implementation in hardware through various activities.

- Performed Signal Integrity and EMC analysis on DDR2/3 interfaces and other critical interfaces to deliver board routing guidelines to hardware team.
- Supported field application team with customer related issues.
- Implemented Power Integrity analysis methodology for mixed-signal chips including SerDes and parallel DDR3 interfaces by developing power delivery requirements through simulations with Speed2K and SiWave resulting in target impedance profiles

SENIOR HARDWARE ENGINEER – Intel – Hillsboro, OR – Oct 2004 – Sept 2006

Worked in a hardware design team creating products for set top boxes and digital televisions as main Signal Integrity and EMC resource across hardware and silicon design teams. Performed hardware and embedded design activities for multiple products. This role started out as a contract position and turned into a full-time position.

- Worked with PCB designers in the group to ensure Signal Integrity goals were met from PCB stackup design through topology selection and routing. Generated platform design guidelines for all interfaces including PCI Express, HDMI, and DDR3 through Signal Integrity simulation for noise and timing margin.
- System architecture implementation and component evaluation for platform performance goals
- PCB Schematics and Layout Ex. Designed front panel interface for PCB board using Cadence Allegro PCB toolset
- Assisted with lab debugging/bring-up activities

SENIOR HARDWARE ENGINEER – Sun Microsystems – Burlington, MA – April 2003 – Sep 2004

Worked in hardware team supporting development of blade servers for server market. Hardware design and analysis of systems including power distribution and electrical interfaces.

- Analyzed systems for Signal Integrity and EMI in blade server market
- Provided board layout rules to meet specified timing and noise margins
- Lab verification of boards using test equipment and correlation to simulation to ensure design margin

APPLICATION ENGINEER – National Semiconductor – Portland, ME – Mar 2002 – April 2003

Application engineer with a focus on Signal Integrity supporting communication and interface product lines including LVDS. Worked with team members to do PCB evaluation boards, bench testing, and support customers.

- Worked closely with circuit designers to define buffer IO characteristics for optimal analog performance
- Supported customer designs with PCB Signal Integrity simulation and routing recommendations
- Created and verified IBIS behavioral models for multiple business units with focus on high-speed LVDS products including SerDes
- Performed pre-layout simulation and analysis on test and evaluation boards, post-layout analysis including lab verification using TDR equipment

APPLICATION ENGINEER – Fairchild Semiconductor – Portland, ME – Jan 2001 – Jan 2002

Member of the applications group supporting customers for logic and interface products. Performed bench evaluations, created PCB reference designs, generated data sheets, and supported customers.

- Circuit simulation support for design group on analog interface products
- Provided SPICE and IBIS behavioral models to customers for logic and interface products including GTLP and LVDS
- Wrote perl scripts and Java programs to help automate simulation model generation process
- Supported customer signal integrity issues through simulation and lab verification of high-speed backplanes and interconnects

Education

B.S. ELECTRICAL ENGINEERING – Digital Signal Processing (DSP) Concentration - University of Maine – Orono, ME -2000